

Amendments to the Claims:

This listing of claims will replace all prior version, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method of minimizing a circuit element interference and stabilizing a performance of a circuit element within a Time Division Duplex (TDD) transceiver, which comprises:

providing a medium for a communication signal propagating back and forth through the medium;

constructing an analog circuit for receiving and transmitting the communication signal through the medium at a time, and for modulating and demodulating the communication signal during a communication signal receiving and transmitting process;

constructing a digital circuit for digital signal processing;

constructing an analog-to-digital (A/D) interface and a digital-to-analog (D/A) interface so that the interfaces couples the analog circuit and the digital circuit together;

providing a first ground reference so that all ground references of circuit elements in the analog circuit, in the A/D interface, and in the D/A interface are connected to the first ground reference;

providing a second ground reference so that all ground references of circuit elements in the digital circuit are grounded to the second ground reference;

providing a switch for transmitting or receiving the communication signal in
different time periods;

providing a down-converter for converting the received communication signal to a
baseband signal; providing an up-converter for converting a baseband
signal to a radio frequency signal;

constructing a synthesizer coupled to a baseband processor, comprising a
voltage controller oscillator to provide the down-converter and the up-
converter with a base frequency of signal so that the received and
baseband communication signals are demodulated and modulated,
respectively; and

providing a joint clock source for supplying clock pulses to the analog circuit, the
digital circuit, the A/D interface, and the D/A interface, wherein the joint
clock source has a ground reference directly connecting to the first
ground reference and without directly connecting to the second ground
reference.

2. (Original) The method of claim 1, wherein the medium is an antenna and the
communication signal propagates through the air.

3. (Original) The method of claim 1, wherein the medium is a communication wire
where the communication signal propagates through the wire.

4. (Original) The method of claim 1, wherein the joint clock source is a crystal oscillator.

5. (Canceled)

6. (Currently amended) The method of claim 1, where in the constructing digital circuit step further comprises: ~~providing baseband processor for digital signal processing;~~ and providing a media access control (MAC) unit.

7. (Original) The method of claim 1, wherein the A/D interface is an analog-to-digital convertor.

8. (Original) The method of claim 1, wherein the D/A interface is a digital-to-analog convertor.

9. (Currently amended) A circuit architecture for minimizing a circuit element interference and stabilizing a performance of a circuit element within a TDD transceiver, which comprises:

a medium within which a communication signal propagates through;

an analog circuit for receiving and transmitting the communication signal in

different time periods, and for modulating and demodulating the

communication signal during a communication signal transmitting and

receiving process;

a digital circuit for digital signal processing; an A/D interface circuit and a D/A interface circuit for coupling the analog circuit and the digital circuit together;

a first ground reference on which all ground references of circuit elements of the analog circuit, the A/D interface circuit, and the D/A interface circuit are connected together;

a second ground reference on which all ground references of circuit elements of the digital circuit are connected together;

a switch for transmitting or receiving the communication signal in different time periods;

a down-converter for converting the received communication signal to a baseband signal;

an up-converter for converting a baseband signal to a radio frequency signal;

a synthesizer coupled to a baseband processor, comprising a voltage controller oscillator to provide the down-converter and the up-converter with a base frequency of signal so that the received and baseband communication signals are demodulated and modulated, respectively; and

a joint clock source to supply clock pulses to the analog circuit, the digital circuit, the A/D interface circuit, and the D/A interface circuit, and to have a ground reference of the joint clock source directly connected to the first ground reference and not directly connected to the second ground reference.

10. (Original) The circuit architecture of claim 9, wherein the medium is an antenna and the communication signal propagates through the air.

11. (Original) The circuit architecture of claim 9, wherein the medium is a communication wire where the communication signal propagates through the wire.

12. (Original) The circuit architecture of claim 9, wherein the joint lock source is a crystal oscillator.

13. (Cancel)

14. (Currently amended) The circuit architecture of claim 9, wherein the digital circuit further comprises: ~~a baseband processor for digital signal processing;~~ and a media access control (MAC) unit.

15. (Original) The circuit architecture of claim 9, wherein the A/D interface is an analog-to-digital convertor.

16. (Original) The circuit architecture of claim 9, wherein the D/A interface is a digital-to-analog convertor.